IN THE CLAIMS

The following is a complete listing of the claims, and replaces all earlier versions and listings.

1. (currently amended) A method for manufacturing a printed circuit board element, ~~wherein starting from~~ comprising the steps of:

providing a printed circuit board substrate [[(12)]] with at least one conductor layer; [[(13),]]

structuring the [[this]] conductor layer; ~~is structured as well as~~

roughening ~~roughened~~ the whole structured conductor layer in the surface area;

applying ~~and metal (16) is applied thereon characterised in that~~ a noble metal layer ~~(16) is applied~~ on the whole structured, roughened conductor layer [[(13)]], ~~wherein~~ the surface of the noble metal layer [[is]] being provided with a corresponding roughness; and [[(8')]]

applying at least one electric PTF component in the area of the surface-roughened noble metal layer by imprinting.

2. (canceled)

3. (canceled)

4. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the surface of the conductor layer ~~(13)~~ is roughened by ionic etching.

5. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the surface of the conductor layer ~~(13)~~ is roughened by mechanical processing.

6. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the surface of the conductor layer ~~(13)~~ is roughened by electroplating.

7. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the noble metal layer ~~(16)~~ is applied on the conductor layer ~~(13)~~ with a thickness of between 0.02 µm and 1 µm~~, preferably 0.02 µm and 0.5 µm~~.

8. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the noble metal layer ~~(16)~~ is applied on the conductor layer ~~(13)~~ in a chemical-currentless manner.

9. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the noble metal layer ~~(16)~~ is applied on the conductor layer [[(13)]] by electroplating.

10. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the noble ~~metall~~ metal layer ~~(16)~~ is applied on the conductor layer ~~(13)~~ by cathodic evaporation.

11. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein the noble ~~metall~~ metal layer ~~(16)~~ is applied on the conductor layer ~~(13)~~ by sputtering.

12. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein a layer made of at least one metal from the group comprising silver, gold, palladium, and platinum,[[ ]]is used as the noble metal layer [[(16)]].

13. (canceled)

14. (currently amended) ~~A~~ The method according to claim ~~13~~ 1, ~~characterised in that~~ wherein the electric component ~~(4)~~ is a resistor~~, e.g. a PTF resistor~~.

15. (currently amended) [[A]] The method according to claim 1, ~~characterised in that~~ wherein, after having applied the noble metal layer [[(16)]] on the roughened conductor layer [[(13)]] ~~as well as, optionally,~~ and after having ~~mounted~~ applied the electric component ~~(4) on the upper side of~~ to the ~~printed circuit board substrate (12)~~ surface-roughened noble metal layer, a further printed circuit board structure [[(1')]] is applied ~~together with the surface roughened noble metal layer (16)~~ and [[thus]] a pressing to a multi layer is ~~yielded~~ performed.

16. (currently amended) [[A]] The method according to claim 1, ~~characterised in that~~ wherein, after having applied the noble metal layer [[(16)]] on the roughened conductor layer ~~(13) as well as, optionally,~~ and after having ~~mounted~~ applied the electric component [[(4)]] on the ~~upper side of the printed circuit board substrate (12)~~ surface-roughened noble metal layer, a solder stop mask is mounted ~~together with the surface roughened noble metal layer (16)~~.

17. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that~~ wherein a

printed circuit board substrate ~~(12)~~ with two conductor layers ~~(13, 13')~~ is used, and ~~wherein~~ at least one conductor layer is structured and roughened.

18. (currently amended) ~~A~~ The method according to claim 1, ~~characterised in that,~~ wherein, after having been structured, the conductor layer is roughened in the surface area.

19. (currently amended) A printed circuit board element comprising:

a printed circuit board substrate with at least one ~~structured~~ conductor layer, the conductor layer being structured, and the whole structured layer being ~~(13) on a substrate (12), which substrate has a~~ roughened in the surface [[(8),]] area;

a noble ~~and with~~ metal [[(16)]] layer on the whole structured, roughened conductor layer [[(13)]], ~~characterised in that a surface-rough~~ the surface of the noble metal layer ~~(16) is applied on the whole roughened conductor layer (13) and serves as contact promoting and stabilizing layer, on the one hand, and as adherence promoting layer, on the other hand~~ having a corresponding roughness; and

at least one imprinted electric PTF component in the area of the surface-roughened noble metal layer.

20. (currently amended) [[A]] The printed circuit board element according to claim 19, ~~characterised in that~~ wherein a further printed circuit board structure ~~(1')~~ is provided on the surface-rough noble layer [[(16),]] forming a multilayer ~~configuration~~.

21. (currently amended) [[A]] The printed circuit board element according to claim 19,

~~characterised in that~~ wherein a solder stop mask is mounted on to the surface-rough noble metal layer [[(16)]].

22. (canceled)

23. (currently amended) [[A]] The printed circuit board element according to claim 22, ~~characterised in that~~ wherein the electric component [[(4)]] is a resistor~~, e.g. a PTF resistor~~.

24. (canceled)

25. (currently amended) [[A]] The printed circuit board element according to claim 19, ~~characterised in that~~ wherein the noble metal layer [[(16)]] has a thickness of between 0.02 µm and 1 µm~~, preferably 0.02 µm and 0.5 µm~~.

26. (currently amended) [[A]] The printed circuit board element according to claim 19, ~~characterised in that~~ wherein the noble metal layer [[(16)]] has at least one metal selected from the group consisting of silver, gold, palladium, and platinum.

27. (currently amended) [[A]] The printed circuit board element acccording to claim 19, ~~characterised in that~~ wherein the substrate [[(12)]] has two structured conductor layers, ~~(13, 13'), wherein on at least one layer a noble metal layer (16) is applied~~ at least one conductor layer being structured and roughened.

28. (new) The method according to claim 1, wherein the noble metal layer is applied on the conductor layer with a thickness of between 0.02 µm and 0.5 µm.

29. (new) The printed circuit board element according to claim 19, wherein the noble metal layer has a thickness of between 0.02 µm and 0.5 µm.